a control signal receiver to receive a receive control signal;

a decoder to decode the receive control signal comprising on one half of a cycle of the second clock signal a receive data valid signal or a carrier sense signal and on the other half of the cycle of the second clock signal a receive error signal; and

a data signal receiver to receive a second data signal.

96. (Amended) A network device, comprising:

a clock receiver to receive a first clock signal;

a control signal receiver to receive a transmit control signal;

a decoder to decode the transmit control signal comprising in a half of a cycle of the first clock signal a transmit enable signal and in the other half of the cycle of the first clock signal a transmit error signal;

a data signal receiver to receive a first data signal;

a clock transmitter to transmit a second clock signal;

an encoder to encode a receive control signal comprising on one half of a cycle of the second clock signal a receive data valid signal or a carrier sense signal and on the other half of the cycle of the second clock signal a receive error signal;

a control signal transmitter to transmit the receive control signal; and

a data signal transmitter to transmit a second data signal.

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Please add claims 109 through 148 as follows:

--109. A method of encoding signals for a network device, comprising the steps of:

receiving a clock signal;

forming a transmit control signal comprising in one half of a cycle of the clock signal a transmit enable signal and comprising in the other half of the cycle of the clock signal a transmit error signal;

transmitting the transmit control signal; and

transmitting a data signal.

110. The method of claim 109, wherein when the transmit enable signal is asserted, the data signal comprises one of packet data and symbol error data.

111. The method of claim 110, wherein

when neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, the data signal comprises idle data;

when the transmit enable signal is asserted and the transmit error signal is not asserted in a cycle of the clock signal, the data signal comprises packet data; and

when both the transmit enable signal and the transmit error signal are asserted in a cycle of the clock signal, the data signal comprises symbol error data.

112. The method of claim 111, wherein

when the transmit enable signal is not asserted and the transmit error signal is asserted in a cycle of the clock signal, the data signal comprises one of carrier extension data and carrier extension data with error.

113. The method of claim 109, wherein the clock signal has a frequency of either 2.5 MHz, 25 or 125 MHz.

114. A method of decoding signals for a network device, comprising the steps of:

transmitting a clock signal;

receiving a transmit control signal;

decoding the transmit control signal comprising in a half of a cycle of the clock signal a transmit enable signal and in the other half of the cycle of the clock signal a transmit error signal; and

receiving a data signal.

115. The method of claim 114, wherein when the transmit enable is asserted, the data signal comprises one of packet data and symbol error data.

116. The method of claim 115, wherein

when neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, the data signal comprises idle data;

when the transmit enable signal is asserted and the transmit error signal is not asserted in a cycle of the clock signal, the data signal comprises packet data; and

when both the transmit enable signal and the transmit error signal are asserted in a cycle of the clock signal, the data signal comprises a symbol error data.

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117. The method of claim 116, wherein

when the transmit enable signal is not asserted and the transmit error signal is asserted in a cycle of the clock signal, the data signal comprises one of carrier extension data and carrier extension data with error.

118. The method of claim 116, wherein the clock signal has a frequency of either 2.5, 25 or 125 MHz.

119. A network device, comprising:

a clock receiver to receive a clock signal;

an encoder to form a transmit control signal comprising in one half of a cycle of the clock signal a transmit enable signal and comprising in the other half of the cycle of the clock signal a transmit error signal;

a control signal transmitter to transmit the transmit control signal encoded by the encoder; and

a data signal transmitter to transmit a data signal.

120. The network device of claim 119, wherein when the encoder forms the transmit control signal on which the transmit enable signal is asserted, the data signal transmitter transmits the data signal comprised of one of packet data and symbol error data.

121. The network device of claim 120, wherein

when the encoder forms the transmit control signal on which neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, the data signal transmitter transmits the data signal comprised of idle data;

when the encoder forms the transmit control signal on which the transmit enable signal is asserted and the transmit error signal is not asserted in a cycle of the clock signal, the data signal transmitter transmits the data signal comprised of packet data; and

when the encoder forms the transmit control signal on which both the transmit enable signal and the transmit error signal are asserted in a cycle of the clock signal, the data signal

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transmitter transmits the data signal comprised of symbol error data.

122. The network device of claim 121, wherein

when the encoder forms the transmit control signal on which the transmit enable signal is not asserted and the transmit error signal is asserted in a cycle of the clock signal, the data signal transmitter transmits the data signal comprised of one of carrier extension data and carrier extension data with error.

123. The network device of claim 119, wherein the clock signal has a frequency of either 2.5, 25 or 125 MHz.

124. A network device, comprising:

a clock transmitter to transmit a clock signal;

a control signal receiver to receive a transmit control signal;

a decoder to decode the transmit control signal comprising in a half of a cycle of the clock signal a transmit enable signal and in the other half of the cycle of the clock signal a transmit error signal; and

a data signal receiver to receive a data signal.

125. The network device of claim 124, wherein

when the decoder the decodes the transmit control signal on which the transmit enable signal is asserted, the data signal receiver receives the data signal comprised of one of packet data and symbol error data.

126. The network device of claim 125, wherein

when the decoder decodes the transmit control signal on which neither the transmit enable signal nor the transmit error

signal are asserted in a cycle of the clock signal, the data signal receiver receives the data signal comprised of idle data;

when decoder decodes the transmit control signal on which the transmit enable signal is asserted and the transmit error signal is not asserted in a cycle of the clock signal, the data signal receiver receives the data signal comprised of packet data; and

when the decoder decodes the transmit control signal on which both the transmit enable signal and the transmit error signal are asserted in a cycle of the clock signal, the data signal receiver receives the data signal comprised of a symbol error data.

127. The network device of claim 126, wherein

when the decoder decodes the transmit control signal on which the transmit enable signal is not asserted and the transmit error signal is asserted in a cycle of the clock signal, the data signal receiver receives the data signal comprised of one of carrier extension data and carrier extension data with error.

128. The network device of claim 124, wherein the clock signal has a frequency of either 2.5, 25 or 125 MHz.

129. A network device, comprising:

means for receiving a clock signal;

means for forming a transmit control signal comprising in one half of a cycle of the clock signal a transmit enable signal and comprising in the other half of the cycle of the clock signal a transmit error signal;

means for transmitting the transmit control signal; and

means for transmitting a data signal.

130. The network device of claim 129, wherein when the transmit enable signal is asserted, the data signal comprises one of packet data and symbol error data.

131. The network device of claim 130, wherein

when neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, the data signal comprises idle data;

when the transmit enable signal is asserted and the transmit error signal is not asserted in a cycle of the clock signal, the data signal comprises packet data; and

when both the transmit enable signal and the transmit error signal are asserted in a cycle of the clock signal, the data signal comprises symbol error data.

132. The network device of claim 131, wherein

when the transmit enable signal is not asserted and the transmit error signal is asserted in a cycle of the clock signal, the data signal comprises one of carrier extension data and carrier extension data with error.

133. The network device of claim 129, wherein the clock signal has a frequency of either 2.5, 25 or 125 MHz.

134. A network device, comprising:

means for transmitting a clock signal;

means for receiving a transmit control signal;

means for decoding the transmit control signal comprising in a half of a cycle of the clock signal a transmit enable signal and in the other half of the cycle of the clock signal a transmit error signal; and

means for receiving a data signal.

135. The network device of claim 134, wherein when the transmit enable is asserted, the data signal comprises one of packet data and symbol error data.

136. The network device of claim 135, wherein

when neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, the data signal comprises idle data;

when the transmit enable signal is asserted and the transmit error signal is not asserted in a cycle of the clock signal, the data signal comprises packet data; and

when both the transmit enable signal and the transmit error signal are asserted in a cycle of the clock signal, the data signal comprises a symbol error data.

137. The network device of claim 136, wherein

when the transmit enable signal is not asserted and the transmit error signal is asserted in a cycle of the clock signal, the data signal comprises one of carrier extension data and carrier extension data with error.

138. The network device of claim 134, wherein the clock signal has a frequency of either 2.5, 25 or 125 MHz.

139. A network device, comprising:

a clock receiver to receive a first clock signal;

an encoder to form a transmit control signal comprising in one half of a cycle of the first clock signal a transmit enable signal and comprising in the other half of the cycle of the first clock signal a transmit error signal;

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a control signal transmitter to transmit the transmit control signal encoded by the encoder;

a data signal transmitter to transmit a first data signal;

a clock receiver to receive a second clock signal;

a control signal receiver to receive a receive control signal;

a decoder to decode the receive control signal comprising on one half of a cycle of the second clock signal a receive data valid signal or a carrier sense signal and on the other half of the cycle of the second clock signal a receive error signal; and

a data signal receiver to receive a second data signal.

140. A network device, comprising:

a clock transmitter to transmit a first clock signal;

a control signal receiver to receive a transmit control signal;

a decoder to decode the transmit control signal comprising in a half of a cycle of the first clock signal a transmit enable signal and in the other half of the cycle of the first clock signal a transmit error signal;

a data signal receiver to receive a first data signal;

a clock transmitter to transmit a second clock signal;

an encoder to encode a receive control signal comprising on one half of a cycle of the second clock signal a receive data valid signal or a carrier sense signal and on the other half of the cycle of the second clock signal a receive error signal;

a control signal transmitter to transmit the receive control signal; and

a data signal transmitter to transmit a second data signal.

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141. The method of claim 109, further comprising the step of inband signaling when neither the transmit enable signal nor the

transmit error signal are asserted in a cycle of the clock signal.

142. The method of claim 114, further comprising the step of inband signaling when neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal.

143. The network device of claim 119, wherein when the encoder forms the transmit control signal on which neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, then the encoder performs inband signaling.

144. The network device of claim 124, wherein when the decoder decodes the transmit control signal on which neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, then the decoder performs inband signaling.

145. The network device of claim 129, wherein when the means for forming forms the transmit control signal on which neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, then the means for forming forms inband signaling.

146. The network device of claim 134, wherein when the means for decoding decodes the transmit control signal on which neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, then the means for decoding performs inband signaling.

147. The network device of claim 124, wherein when the decoder decodes the transmit control signal on which neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, then the decoder performs inband signaling.

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148. The network device of claim 134, wherein when the means for decoding decodes the transmit control signal on which neither the transmit enable signal nor the transmit error signal are asserted in a cycle of the clock signal, then the means for decoding performs inband signaling.--

REMARKS

Claims 1 - 148 are presented for examination. Claims 95 and 96 have been amended to improve their form, and claims 109 - 148 having been added to present claims directed to different aspects of the invention. The amendments and addition of claims have not been made to overcome prior art.

Favorable consideration is respectfully requested.

Respectfully submitted,

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Date: 6/30/00

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